AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A device configured for use in a computer system, comprising:

an indicator configured to indicate when the computer system is in a secure ~~first~~ operating mode;

a first timer configured to indicate a duration in which the indicator is active; and

control logic coupled to receive the duration from the first timer, wherein the control logic is configured to provide a control signal upon the duration reaching a predetermined value.

2. (Original) The device of claim 1, wherein the device includes a bridge.

3. (Original) The device of claim 2, wherein the bridge includes a south bridge.

4. (Canceled)

5. (Currently Amended) The device of claim 1 [[4]], wherein the secure operating mode includes system management mode (SMM).

6. (Currently Amended) The device of claim 1 [[4]], wherein the control signal is configured to indicate that the computer system should exit the secure operating mode.

7. (Original) The device of claim 1, wherein the predetermined value less than about 2 seconds.

8. (Original) The device of claim 7, wherein the predetermined value is not substantially less than 200 milliseconds.

9. (Original) The device of claim 1, wherein the predetermined value is set by software or firmware executing in the device.

10. (Original) The device of claim 1, further comprising:

a second timer configured to indicate a duration since the control signal has been provided;

wherein the control logic is further coupled to receive an indication from the second timer of the duration, wherein the control logic is further configured to provide a second control signal upon the duration since the control signal has been provided reaching a second predetermined value.

11. (Original) The device of claim 10, wherein the second control signal is configured to indicate that the computer system should enter the secure operating mode.

12. (Currently Amended) A computer system, comprising:

a processor; and

a device coupled to the processor, wherein the device includes:

an indicator configured to indicate when the processor is in a secure ~~first~~ operating mode;

a first timer configured to indicate a duration in which the indicator is active; and

control logic coupled to receive the duration from the first timer, wherein the control logic is configured to provide a control signal to the processor upon the duration reaching a predetermined value.

13. (Original) The computer system of claim 12, wherein the device comprises a bridge.

14. (Original) The computer system of claim 13, wherein the bridge comprises a south bridge.

15. (Canceled)

16. (Currently Amended) The computer system of claim 12 [[15]], wherein the secure operating mode includes SMM.

17. (Currently Amended) The computer system of claim 12 [[15]], wherein the control signal is configured to indicate that the processor should exit the secure operating mode.

18. (Original) The computer system of claim 12, wherein the predetermined value less than about 2 seconds.

19. (Original) The computer system of claim 18, wherein the predetermined value is not substantially less than 200 milliseconds.

20. (Original) The computer system of claim 12, wherein the predetermined value is set by software or firmware executing in the device.

21. (Original) The computer system of claim 12, wherein the device further comprises:

a second timer configured to indicate a duration since the control signal has been provided;

wherein the control logic is further coupled to receive an indication from the second timer of the duration, wherein the control logic is further configured to provide a second control signal upon the duration since the control signal has been provided reaching a second predetermined value.

22. (Original) The computer system of claim 21, wherein the second control signal is configured to indicate that the processor should enter the secure operating mode.

23. (Original) The computer system of claim 22, wherein the device further comprises:

a register coupled to receive a jump address for an interrupt, wherein the jump address corresponds to the processor entering the secure operating mode.

24. (Original) The computer system of claim 23, wherein the interrupt comprises an SMI, wherein the secure operating mode comprises SMM.

25. (Currently Amended) A method for operating a computer system, the method comprising:

determining if the computer system is in a secure ~~first~~ operating mode;

initiating a first timer if the computer system is in the first operating mode;

determining if the first timer has reached a predetermined value; and

asserting a control signal if the first timer has reached the predetermined value.

26. (Currently Amended) The method of claim 25, wherein determining if the computer system is in a secure ~~first~~ operating mode includes determining if the computer system is in system management mode, and wherein asserting a control signal if the first timer has reached the predetermined value includes executing an RSM instruction before an SMI handler exits the system management mode.

27. (Original) The method of claim 26, further comprising:

issuing an SMI request;

the computer system entering system management mode; and

the SMI handler servicing the SMI request;

wherein executing an RSM instruction before an SMI handler exits the system management mode occurs while the SMI handler is servicing the SMI request.

28. (Currently Amended) A method for operating a computer system, the method comprising:

step for determining if the computer system is in a secure ~~first~~ operating mode;

step for initiating a first timer if the computer system is in the secure ~~first~~ operating mode;

step for determining if the first timer has reached a predetermined value; and

step for asserting a control signal if the first timer has reached the predetermined value.

29. (Currently Amended) The method of claim 28, wherein the step for determining if the computer system is in a secure ~~first~~ operating mode includes step for determining if the computer system is in system management mode, and wherein the step for asserting the control signal if the first timer has reached the predetermined value includes step for executing an RSM instruction before an SMI handler exits the system management mode.

30. (Original) The method of claim 29, further comprising:

step for issuing an SMI request;

step for the computer system entering system management mode; and

step for the SMI handler servicing the SMI request;

wherein the step for executing an RSM instruction before an SMI handler exits the system management mode occurs while the SMI handler is servicing the SMI request.

31. (Currently Amended) A computer readable program storage device encoded with instructions that, when executed by a computer system, performs a method of operating the computer system, the method comprising:

determining if the computer system is in a secure ~~first~~ operating mode;

initiating a first timer if the computer system is in the secure ~~first~~ operating mode;

determining if the first timer has reached a predetermined value; and

asserting a control signal if the first timer has reached the predetermined value.

32. (Original) The computer readable program storage device of claim 31, wherein determining if the computer system is in a secure ~~first~~ operating mode includes determining if the computer system is in system management mode, and wherein asserting a control signal if the first timer has reached the predetermined value includes executing an RSM instruction before an SMI handler exits the system management mode.

33. (Original) The computer readable program storage device of claim 32, the method further comprising:

causing an SMI request to be issued;

wherein executing an RSM instruction before an SMI handler exits the system management mode occurs while the SMI handler is servicing the SMI request.

34. (Withdrawn) A method for operating a computer system, the method comprising:

executing at least one instruction in a secure operating mode;

exiting the secure operating mode; and

entering the secure operating mode prior to the computer system reloading a previous state not in the secure operating mode.

35. (Withdrawn) The method of claim 34, further comprising:

executing at least one instruction in an operating mode other than the secure operating mode;

storing the previous state of the computer system in the operating mode other than the secure operating mode; and

entering the secure operating mode.

36. (Withdrawn) The method of claim 34, wherein exiting the secure operating mode comprises exiting the secure operating mode prior to the end of a code routine.

37. (Withdrawn) The method of claim 34, wherein the secure operating mode is system management mode;

wherein exiting the secure operating mode comprises executing an RSM instruction before an SMI handler exits the system management mode; and

wherein entering the secure operating mode comprises issuing an SMI request before the previous state is loaded.

38. (Withdrawn) A method for operating a computer system, the method comprising:

step for executing at least one instruction in a secure operating mode;

step for exiting the secure operating mode; and

step for entering the secure operating mode prior to the computer system reloading a previous state not in the secure operating mode.

39. (Withdrawn) The method of claim 38, further comprising:

step for executing at least one instruction in an operating mode other than the secure operating mode;

step for storing the previous state of the computer system in the operating mode other than the secure operating mode; and

step for entering the secure operating mode.

40. (Withdrawn) The method of claim 38, wherein the step for exiting the secure operating mode comprises step for exiting the secure operating mode prior to the end of a code routine.

41. (Withdrawn) The method of claim 38, wherein the secure operating mode is system management mode;

wherein the step for exiting the secure operating mode comprises step for executing an RSM instruction before an SMI handler exits the system management mode; and

wherein the step for entering the secure operating mode comprises step for issuing an SMI request before the previous state is loaded.

42. (Withdrawn) A computer readable program storage device encoded with instructions that, when executed by a computer system, performs a method of operating the computer system, the method comprising:

executing at least one instruction in a secure operating mode;

exiting the secure operating mode; and

entering the secure operating mode prior to the computer system reloading a previous state not in the secure operating mode.

43. (Withdrawn) The computer readable program storage device of claim 42, the method further comprising:

executing at least one instruction in an operating mode other than the secure operating mode;

storing the previous state of the computer system in the operating mode other than the secure operating mode; and

entering the secure operating mode.

44. (Withdrawn) The computer readable program storage device of claim 42, wherein exiting the secure operating mode comprises exiting the secure operating mode prior to the end of a code routine.

45. (Withdrawn) The computer readable program storage device of claim 42, wherein the secure operating mode is system management mode;

wherein exiting the secure operating mode comprises executing an RSM instruction before an SMI handler exits the system management mode; and

wherein entering the secure operating mode comprises issuing an SMI request before the previous state is loaded.